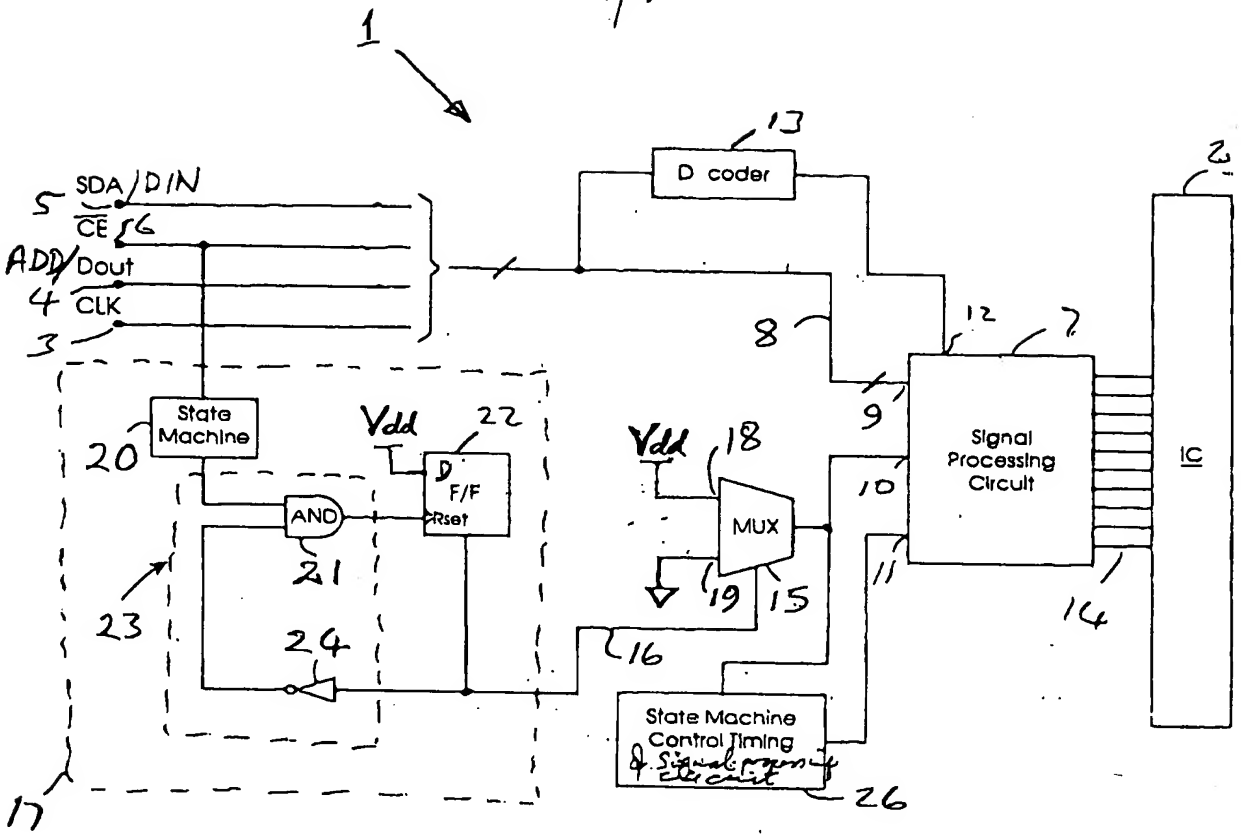
1
SDA/DIN
CE
ADD/Dout
CLK
5
6
4
3
D coder
13
2
8
12
7
9
10
11
14
IC
Signal Processing Circuit
State Machine
20
Vdd
22
D F/F
Rset
AND
21
23
24
Vdd
18
MUX
19
15
16
State Machine Control Timing & Signal Processing Circuit
26
17

FIG 1

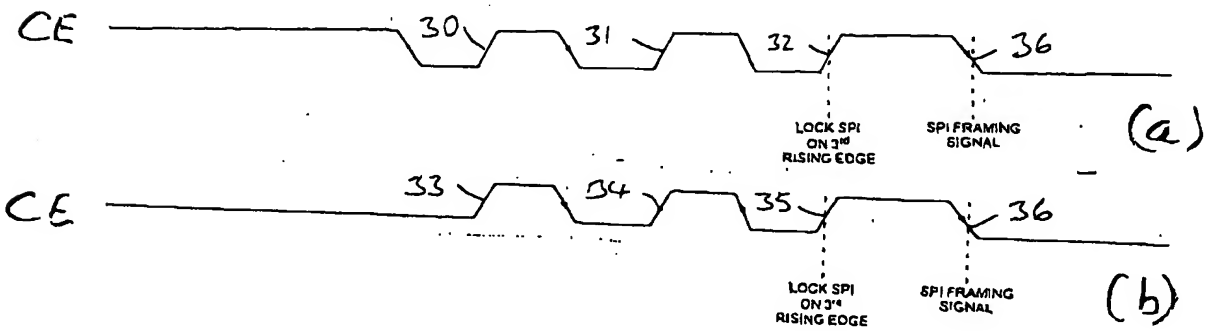
CE
30
31
32
36
LOCK SPI ON 3rd RISING EDGE
SPI FRAMING SIGNAL
(a)
CE
33
34
35
36
LOCK SPI ON 3rd RISING EDGE
SPI FRAMING SIGNAL
(b)

FIG 2

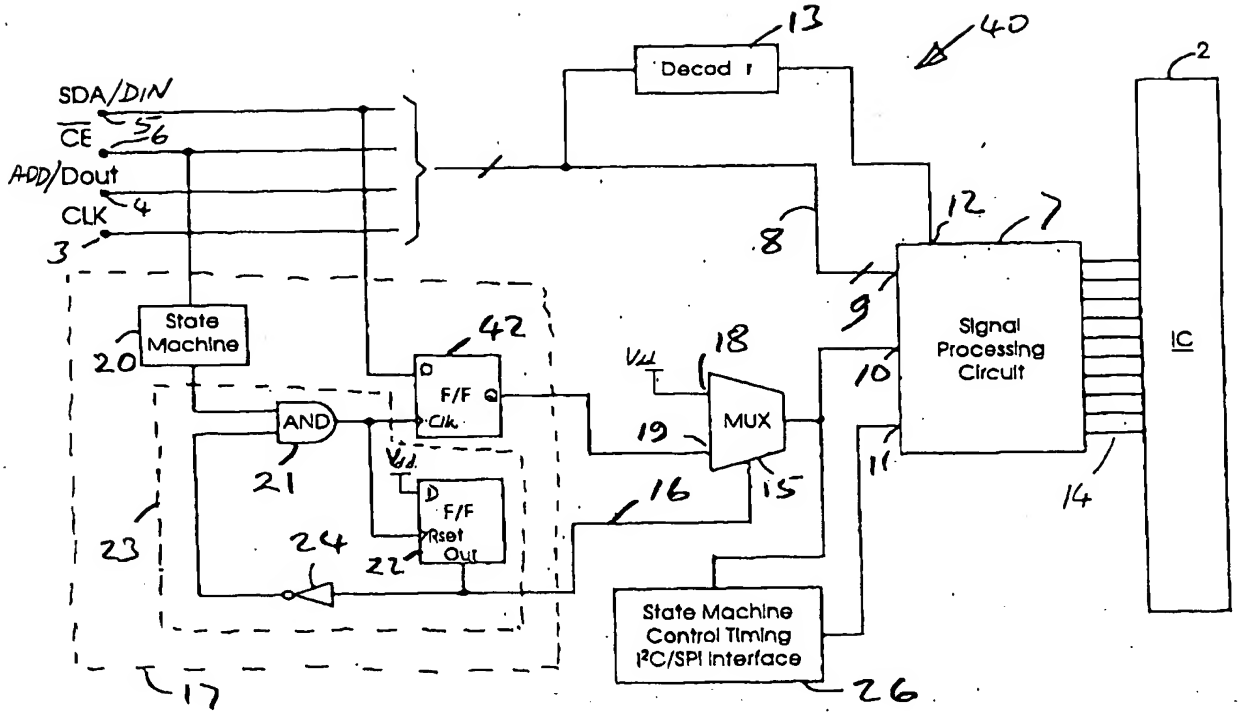
SDA/DIN
CE
ADD/Dout
CLK
3
5
6
4
Decod r
13
40
2
8
12
7
9
10
11
14
Signal Processing Circuit
IC
State Machine
20
42
D
F/F
Q
Clk
AND
21
Vdd
18
MUX
19
15
16
23
24
22
Rset
Out
State Machine Control Timing I²C/SPI Interface
26
17

FIG 3

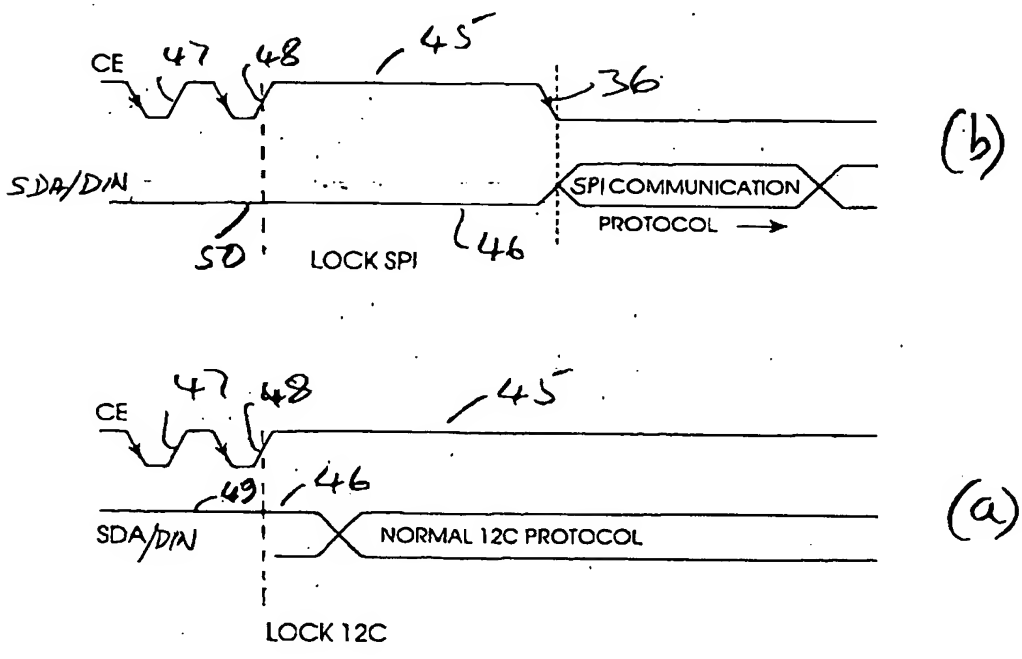
CE
47
48
45
36
SDA/DIN
SPI COMMUNICATION
PROTOCOL
(b)
50
LOCK SPI
46
CE
47
48
45
49
46
SDA/DIN
NORMAL 12C PROTOCOL
(a)
LOCK 12C

FIG 4